What is claimed is:

1. A semiconductor integrated circuit comprising:

an adjusted circuit in which a first bias current flows, a slew rate of said adjusted circuit being dependent on said first bias current:

a replica circuit of said adjusted circuit in which a second bias current flows, a value of said second bias current being substantially equal to that of said first bias current;

an evaluation circuit configured to repeat processing, said processing including: resetting an output thereof; obtaining a difference between first and second values of an output of said replica circuit given times, said first and second values being respective ones at respective times when first and second time intervals has elapsed after a given value having been step-inputted to said replica circuit; and successively summing said differences;

a comparator circuit for comparing a value obtained by said successively summing with a reference value; and

a bias adjustment circuit for changing said second bias current according to a comparison result of said comparator circuit at every said given times.

2. The semiconductor integrated circuit of claim 1, wherein said evaluation circuit comprises:

a subtraction/integration circuit integrating each

difference between said first output value and said second output value; and

a control circuit;

wherein said control circuit is configured to

(1) cause an integral of said subtraction/integration circuit to be reset;

(2) repeat processing said given times, said processing including: causing said replica circuit to be reset; next causing said given value to be step-inputted to said replica circuit; causing said output of said replica circuit as said first value to be provided to said subtraction/integration circuit after or till said first time interval has elapsed from said step-inputting; next causing said replica circuit to be reset; next said given value to be step-inputted to said replica circuit; causing said output of said replica circuit as said second value to be provided to said subtraction/integration circuit after or till said second time interval has elapsed from said step-inputting; and

repeat the processing of said (1) and (2).

3. The semiconductor integrated circuit of claim 2,

wherein said bias adjustment circuit is configured to step up said bias current in response to judgment that said successively summed value is larger than said reference value by said comparator circuit,

wherein said control circuit is configured to cease its operation in response to judgment that said successively summed value is smaller than said reference value.

4. The semiconductor integrated circuit of claim 2,

wherein said bias adjustment circuit is configured to step down said bias current in response to judgment that said successively summed value is smaller than said reference value by said comparator circuit, and

wherein said control circuit is configured to cease its operation in response to judgment that said successively summed value is larger than said reference value.

5. The semiconductor integrated circuit of claim 2,

wherein said bias adjustment circuit is configured to step down said bias current in response to judgment that said successively summed value is smaller than said reference value by said comparator circuit, and step up said bias current in response to judgment that said successively summed value is larger than said reference value by said comparator circuit,

wherein said control circuit is configured to cease its operation in a case where an absolute value of a difference between said successively summed value and said reference value is smaller than a given value.

6. The semiconductor integrated circuit of claim 3,

wherein said replica circuit has an inverting output

and a non-inverting output,

wherein said subtraction/integration circuit comprises:

an operational amplifier circuit having an inverting input, a non-inverting input, an inverting output and a non-inverting output;

a first integrating capacitor connected between said inverting input and non-inverting output of said operational amplifier circuit;

a second integrating capacitor connected between said non-inverting input and inverting output of said operational amplifier circuit;

a reset switching circuit for resetting electric charges on said first and second integrating capacitors;

first and second sampling capacitors; and

a switching circuit for selectively charging said first and second sampling capacitors or said second and first capacitors by said inverting output and non-inverting output, respectively, of said replica circuit, and thereafter transferring electric charges on said first and second sampling capacitors to said first and second integrating capacitors, respectively.

7. The semiconductor integrated circuit of claim 6, wherein said subtraction/integration circuit further comprises:

a first polarity changeover circuit for connecting first ends of said first and second integrating capacitors to respective said inverting and non-inverting inputs of said operational amplifier circuit to change into a parallel connection state, or connecting said first ends of said first and second integrating capacitors to respective said non-inverting and inverting inputs of said operational amplifier circuit to change into a cross connection state, selectively; and

a second polarity changeover circuit for connecting second ends of said first and second integrating capacitors to respective said non-inverting and inverting outputs of said operational amplifier circuit to change into a parallel connection state, or connecting said second ends of said first and second integrating capacitors to respective said inverting and non-inverting inputs of said operational amplifier circuit to change into a cross connection state, selectively.

8. The semiconductor integrated circuit of claim 7, wherein said control circuit alternately repeats a first period for causing both said first and second polarity changeover circuits to be in said parallel connection state and a second period for causing both said first and second polarity changeover circuits to be in said cross connection state, and performs said processing in said step (2) once in

each of said first and second periods.

9. The semiconductor integrated circuit of claim 1, wherein said adjusted circuit comprises an operational amplifier circuit.

10. The semiconductor integrated circuit of claim 2, wherein said adjusted circuit comprises an operational amplifier circuit.

11. The semiconductor integrated circuit of claim 3, wherein said adjusted circuit comprises an operational amplifier circuit.

12. The semiconductor integrated circuit of claim 4, wherein said adjusted circuit comprises an operational amplifier circuit.

13. The semiconductor integrated circuit of claim 5, wherein said adjusted circuit comprises an operational amplifier circuit.

14. The semiconductor integrated circuit of claim 6, wherein said adjusted circuit comprises an operational amplifier circuit.

15. The semiconductor integrated circuit of claim 7, wherein said adjusted circuit comprises an operational amplifier circuit.

16. The semiconductor integrated circuit of claim 8, wherein said adjusted circuit comprises an operational amplifier circuit.

17. The semiconductor integrated circuit of claim 9, wherein said adjusted circuit further comprises a switched capacitor circuit connected to an input stage of said operational amplifier circuit.

18. The semiconductor integrated circuit of claim 10, wherein said adjusted circuit further comprises a switched capacitor circuit connected to an input stage of said operational amplifier circuit.

19. The semiconductor integrated circuit of claim 11, wherein said adjusted circuit further comprises a switched capacitor circuit connected to an input stage of said operational amplifier circuit.

20. The semiconductor integrated circuit of claim 12, wherein said adjusted circuit further comprises a switched capacitor circuit connected to an input stage of said operational amplifier circuit.